REMARKS/ARGUMENTS

Claims 1-16 are pending and all claims are rejected. Claims 1, 5, 8, 11, and 14 are amended as is explained in further detail below. Claim 1 has also been amended to correct an informality. Claim 16 has been cancelled. New claims 17-20 are presented for examination. Further consideration is respectfully requested.

The drawings stand objected to under 37 CFR 1.83(a). Specifically, the Examiner has asserted that the limitation of "driving a gate terminal of [at] least one element of said output stage to a level above that of said supply voltage source" is not shown in the drawing figures.

The Examiner has also asserted that the specification lacks the description of the limitation of claims 1, 4, 5, 7, 14, and 16 of "driving a gate terminal of [at] least one element of said output stage to a level above/higher than that of said supply voltage source".

In response, new drawing FIG. 3 is submitted that includes all of the claim limitations. No new matter has been introduced into drawing FIG. 3. Support for the new drawing FIG. 3 is found, *inter alia*, in the specification at page 3, lines 9-14, page 4, lines 8-12, page 4, lines 3-33, and page 10, lines 14-21, as well as in claims 1, 4, 5, 7, 14, and 16.

The Examiner's assertion that "driving a voltage below VSS and driving a voltage above VCC to the gate terminal of the output stage transistors has very different concepts and required different circuitry implementation" is respectfully traversed. The circuit for driving the voltage above VCC is topologically identical to the circuitry that is shown in FIG. 2, except for circuit 202. To implement the driving circuit at the transistor level, one would only have to "flip" the circuit shown in FIG. 2, exchange the power supply connections, and substitute N-channel transistors for P-channel transistors, and vice versa. It is deemed that this type of circuit "flipping" is well known in the art of CMOS circuits and can be easily implemented by persons having ordinary skill in the art. For example, any current mirror circuit coupled to

ground for sinking output current can be easily re-designed as a current mirror circuit coupled to VCC for sourcing output current using the well-known technique described above. No changes to the circuit topology need be made to implement the second embodiment of the current mirror.

At least claims 1-6, 8, 9, 11, 12, and 14 stand rejected under 35 USC 102(b) as being anticipated by Arimoto, US Patent No. 6,100,563. It is assumed that claim 13 is also rejected under 35 USC 102(b). The rejection of claims 1, 5, 8, 11, and 14, as amended, is respectfully traversed. Independent claims 1, 5, 8, 11, and 14 have been amended to recite that the output stage is directly coupled between the supply voltage source and the reference voltage source. This limitation is not taught in Arimoto, where at least one switch is coupled between the output stage and supply voltage source or reference voltage source. See, for example, FIGS. 2 and 10 of Arimoto. No new matter has been introduced into claims 1, 5, 8, 11, and 14. Support for the "direct" limitation in claims 1, 5, 8, 11, and 14 is found, *inter alia*, in the specification at page 7, lines 24-31 and page 9, lines 15-16, and in the brief description of FIG. 2.

The direct connection as taught and claimed in the present application allows certain advantages that are not possible with indirect switched connection taught in Arimoto. As taught in the present specification at page 9, lines 24-32:

> In Active Mode, however, the switching speed of the output stage 224 is not impacted, and the preceding stage 220 may be made smaller than the output stage 224 of on the order of approximately one third to one fifth the size. Therefore, the current surge through the power-gate transistor 212 will be relatively small compared to that through transistor 112 in the conventional approach of Fig. 1. (emphasis added)

The remaining dependent claims are also deemed to be allowable as being dependent upon amended claims 1, 5, 8, 11, or 14, as now amended for the reasons given above.

Claims 7 and 10 stand rejected under 35 USC 103(a) as being unpatentable over Arimoto. The rejection of claims 7 and 10 is respectfully traversed. Claim 7 is deemed to be allowable as being dependent upon allowable base claim 5, as amended, for the reasons given above. Claim 10 is deemed to be allowable as being dependent upon allowable base claim 8, as amended, for the reasons given above.

New claims 17-20 are presented for examination, and deemed to be allowable for the reasons given above. The recitation of a "common gate terminal" is deemed to be fully supported by drawing FIG. 2. Note that the gates of the P-channel output transistor and the N-channel transistor in the output stage are coupled together at common gate terminal 232. No new matter is deemed to be introduced into new claims 17-20.

In view of all of the above, claims 1-15 and 17-20 are now believed to be allowable and the case in condition for allowance which action is respectfully requested. Should the Examiner be of the opinion that a telephone conference would expedite the prosecution of this case, the Examiner is requested to contact Applicants' attorney at the telephone number listed below.

No fee is believed due for this submittal. However, any fee deficiency associated with this submittal may be charged to Deposit Account No. 50-1123.

Respectfully submitted,

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